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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/265,119	03/09/1999	MAURIZIO PERI	856063.579	4151

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EXAMINER	
SHARON, AYAL I	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 10/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/265,119	PERI ET AL.	
	Examiner	Art Unit	
	Ayal I Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 10-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-8 and 21-27* is/are allowed.

6)☒ Claim(s) *10-12 and 16* is/are rejected.

7)☒ Claim(s) *13-15 and 17-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 March 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. Claims 1-8 and 10-24 of U.S. Application 09/265,119 were pending before the entry of the present amendment, filed on 06/30/2004. The application was originally filed on 03/09/1999, and has a Foreign Priority filing date of 9/30/98. Claims 1, 5, 8, 10-16 and 21-24 were amended in the present amendment, and new claims 25-27 were added. Claim 9 was previously cancelled.

Drawings

2. This application has been filed with informal drawings (Figs. 1 and 18) which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Claim Interpretations

3. In paper #7, Examiner interpreted a "Flash" memory structure as being a "flash EEPROM" as described in Brigati et al., U.S. Patent 6,011,717, Col. 1, lines 24-31. Examiner also interpreted "Flash EPROM" as being a set of devices that include "flash EEPROM".
4. Examiner is providing the following definitions in order to clarify the definitions of the terms.

- According to the Lee '923 et al., U.S. Patent 5,777,923 (col. 1, lines 13-19):

  "In essence, a flash memory is an electrically erasable programmable read only memories (EEPROM) that supports three operations: read, program and erase."

- According to the Lee '923 et al., U.S. Patent 5,777,923 (col. 1, lines 49-54):

  "Known flash memories have several drawbacks. Some known flash memories perform block program and erase functions to initialize the entire memory into a predetermined state prior to programming the memory with new data. There is no flexibility to select arbitrary words or bits within a block to be efficiently erased or programmed. An example is given in Table 1."

Therefore, Examiner interprets the difference between EEPROM and Flash to be that Flash can only be erased one block at a time, whereas EEPROM enables smaller element sizes to be erased.

5. Applicants note in paper #15, p.8, that "the term of art used for the smallest block that can be erased in a FLASH memory is the term "sector". Examiner agrees with the Applicants that these definitions are substantially the same.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. The prior art used for these rejections is as follows:

- Cappelletti et al., U.S. Patent 6,275,960. (Henceforth referred to as "**Cappelletti**").

8. **Claims 10-12 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Cappelletti.**

9. In regards to Claim 10, Cappelletti teaches the following limitations:

10. A NOR Flash memory device for emulating an EEPROM, comprising:

first and second NOR Flash memory portions each including plural memory blocks with plural memory locations, each of the memory locations sharing an address with a corresponding memory location in each of the blocks of the first and second NOR Flash memory portions, all of the memory locations sharing a same address being a set of memory locations; and
(Cappelletti, especially: col.2, lines 5-35 teaches that all bytes of a given row share the same the same row address;
col.3, lines 33-40 teaches the use of NOR Flash memories;)

a plurality of memory pointers each reflecting which memory block includes a current memory location for a set of memory locations, each set of memory locations including a current memory location;
(Cappelletti, especially: col.3, lines 43-53 teaches "... at least one additional row 16 in which to store parity coeds relative to parity checks of bytes of each row and ... of each column, respectively ...")

a memory controller structured to, in response to receiving a request to write data to a selected address assigned to a selected one of the sets of memory locations, determine from a memory pointer associated with the selected address which memory location in the selected set is a next memory location following the current memory location for the selected set and write the data in the next memory location.
(Cappelletti, especially: Fig.1, item 24 and col.4, lines 16-18)

an internal address bus running inside the memory macrocell;
(Cappelletti, especially: col.2, lines 19-23 teaches that "starting from row '0', all the bytes of the row are read in sequence ..." and "the row address is incremented ... until exhausting all the rows of the sector" and "... the column address is incremented...".)

Examiner finds that it is inherent that there is an internal address bus in the memory macrocell, otherwise it would be impossible to access the specific rows and columns as taught in Cappelletti.

an address counter having an output connected to the internal address bus;
(Cappelletti, especially: col.2, lines 19-23 teaches that "starting from row '0', all the bytes of the row are read in sequence ..." and "the row address

is incremented ... until exhausting all the rows of the sector" and "... the column address is incremented...".)

Examiner finds that it is inherent that there is an address counter connected to the internal address bus, otherwise it would be impossible to access the specific rows and columns as taught in Cappelletti.

a state machine for controlling the address counter, said address counter receiving control signals from the state machine in order to control the loading of hard-coded addresses such that the corresponding pages always share the same non-changeable address.
(Cappelletti, especially: col.4, lines 5-16.)

Examiner finds that the methodology taught in col.4, lines 5-16 of Cappelletti corresponds to a state machine.

10. In regards to Claim 11, Cappelletti teaches the following limitations:

11. The NOR Flash memory device of claim 10 wherein the first and second NOR Flash memory portions are part of first and second memory sectors, the first memory sector including a first set of the plurality of memory pointers associated with the first NOR Flash memory portion and the second memory sector including a second set of the plurality of memory pointers associated with the second NOR Flash memory portion.
(Cappelletti, especially: col.2, lines 50-55)

11. In regards to Claim 12, Cappelletti teaches the following limitations:

12. The NOR Flash memory device of claim 10 wherein each block includes a plurality of memory pages with each memory page including a plurality of the memory locations and each of the memory pointers is a page pointer associated with a respective one of the memory pages.
(Cappelletti, especially: col.2, lines 50-55)

12. In regards to Claim 16, Cappelletti teaches the following limitations:

16. A method of emulating an EEPROM using NOR Flash memory, the method comprising:

dividing the NOR Flash memory into first and second memory sectors each including a plurality of memory blocks, each memory block including plural memory pages each with plural memory locations;
(Cappelletti, especially: col.2, lines 5-35 teaches that all bytes of a given row share the same the same row address;
col.3, lines 33-40 teaches the use of NOR Flash memories;)

assigning to each memory page of the first and second memory sectors a page address that is shared by a corresponding page in each of the memory blocks of the first and second memory sectors wherein such assignment is hard-coded such that the corresponding pages always share the same non-changeable address;

(Cappelletti, especially: col.2, lines 5-35 teaches that all bytes of a given row share the same the same row address;
col.3, lines 33-40 teaches the use of NOR Flash memories;)

in response to a first write instruction to write to a selected page address, writing to a data page of a first memory block of the first memory sector, and updating a state machine to indicate that the first memory block of the first memory sector contains valid data;
(Cappelletti, especially: col.4, lines 5-20, especially the parity bit used in the parity check.)

in response to a second write instruction to write data to the selected page address, writing to a data page of a second memory block of the first memory sector, updating the state machine to indicate that the first memory block of the first memory sector contains invalid data, and updating the state machine to indicate that the second memory block of the first sector contains valid data; and
(Cappelletti, especially: col.4, lines 20-55. The "parity bit value" is the indication in the state machine that the block contains valid or invalid data)

in response to a read instruction to read data from the selected page address, determining from the state machine which memory block contains valid data, and reading the data page corresponding to the memory block containing valid data.
(Cappelletti, especially: col.4, lines 48-49. The "parity check value" is used by the state machine to determine which memory block contains valid or invalid data)

Response to Amendment

Re: Claim Objections

13. Applicants have amended claim 24 in order to correct an informality. The objection to the claim has been withdrawn.

Re: Claim Rejections - 35 USC § 112

14. Applicants have amended claim 1 in a manner which resolves the 35 USC § 112 2nd paragraph rejections of claims 1-7. The rejections of claims 1-7 have been withdrawn.

Re: Claim Rejections - 35 USC § 102

15. Examiner has found the Applicants' arguments in the amendment filed 06/30/2004, on pp.10-11, to be persuasive regarding amended independent claims 10 and 16. The rejections based on the Robinson reference have been withdrawn.

16. New art rejections have been applied, as necessitated by amendment.

Re: Claim Rejections - 35 USC § 103

17. Examiner has found the Applicants' arguments in the amendment filed 06/30/2004, on pp.11-14, to be persuasive regarding amended independent claims 1, 8, 22 and 24, and their dependent claims 2-7, and 21. The rejections based on the Lee '286 and James references have been withdrawn.

Allowable Subject Matter

18. Claims 13-15 and 17-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Examiner's Reasons for Allowance

19. Claims 1-8, and 21-27 are allowed.

20. The following references are discussed in the reasons for allowance of claims 1-8 and 21-17 immediately below:

- Lee, U.S. Patent 5,956,268. (Henceforth referred to as "**Lee '268**").
- James et al., U.S. Patent 5,966,723. (Henceforth referred to as "**James**")

21. Independent claims 1, 8, 22 and 24, and their dependent claims 2-7, and 21 are allowable due to Applicants arguments in the amendment filed 06/30/2004, pp.10-14.

22. In regards to Claim 1, Examiner finds the following argument by the Applicant to be persuasive (see p.12 of the amendment):

> In addition, Lee '268 fails to teach or suggest a device in which the selected number of EEPROM memory cells being emulated is few[er] than the selected number of NOR Flash memory cells. The hypothetical Lee '268 memory device with a single byte sector would not result in the number of emulated EEPROM memory cells being emulated being fewer than the number of NOR Flash memory cells. Rather, there would be a one to one relationship between the number of memory cells emulated and the number being used. Accordingly, it would not result in a device wherein the selected number of EEPROM memory cells being emulated being fewer than the number of NOR Flash memory cells as recited by claim 1.

23. In regards to Claim 8, Examiner finds the following argument by the Applicant to be persuasive (see p.13 of the amendment):

> In addition, Lee '268 and James fail to teach or suggest the recited page updating and swapping. The Examiner admits that Lee '268 does not teach or suggest the page updating and page swapping to another emulated EEPROM sector, but mistakenly asserts that James does. James teaches a method to shift data into or out of the Flash memory device (see e.g., James, col.5, line 10 – col.6, line 12). No mechanism is provided to shift page data to a next block within the memory array. Moreover, such shifting into or out of a memory device does not involve swapping all of the pages of a first sector to a second sector when the first sector is full.

24. In regards to Claim 22, Examiner finds the following argument by the Applicant to be persuasive (see pp.13-14 of the amendment):

> Further, Lee '268 and/or James fail to teach an address counter for tracking and controlling the address at which emulated EEPROM data is stored. James teaches an "Address Register", (see e.g., James, Fig.2, element 6; Fig.2, "To Address Register"; col.4, line 6), as well as a "command/address shift register, (see, e.g., James, Fig.2, element 17; col.5, line 19). These registers are not address counters. It is commonly known in the art that an address counter must include both a storage element as well as means to increment or decrement the storage element. No such means are taught or suggested for incrementing or decrementing the address register or the command/address shift register. Accordingly, these shift registers cannot be the address counters cited by the Examiner.

25. In regards to Claim 24, Examiner finds the following argument by the Applicant to be persuasive (see p.14 of the amendment):

> As further discussed in regards to claim 1, Lee '268 and/or James fail to teach or suggest a device wherein the number of emulated EEPROM bytes comprised substantially fewer memory cells than an entire sector, as recited by claim 24. Accordingly, Lee '268 and/or James do not teach or suggest the features as recited by claim 24.

26. In regards to Claims 6, 14-15 and 23, these claims were indicated as having allowable subject matter in the previous Office Action dated 12/31/2003. They were objected to as being dependent upon rejected base claims 1, 10, and 22. In the present amendment filed on 06/30/2004, amendments were made to independent claims 1, 10, and 22.

27. Claim 23 has been amended to include the pre-amendment limitations of base claim Claim 22. Claim 23 is allowable because none of the cited prior art references, either individually or in combination, expressly teach the following limitation in combination with the other limitations of claim 23:

> "... a state machine coupled to the address counter and coupled for outputting control signals, the address counter receiving control signals from the state machine to control the loading of hard coded addresses in storage

registers which are read and updated by the microcontroller during a reset phase or by the state machine after an EEPROM update wherein said storage registers is a RAM buffer which is coupled for page updating of the EEPROM, the RAM buffer including sufficient storage for storing a page address of the memory array during a page update phase."

28. New Claim 25 contains the limitations of Claim 6. Claim 25 also includes the pre-amendment limitations of Claim 1. Claim 25 is allowable because none of the cited prior art references, either individually or in combination, expressly teach the following limitation in combination with the other limitations of claim 25:

> "... wherein said internal address bus is connected to the input of a RAM buffer which is used for the page updating of the EEPROM including two additional byte for storing a page address during a page updating phase."

29. New Claim 26 contains the pre-amendment limitations of Claim 14. Claim 26 also includes the pre-amendment limitations of Claim 10. Claim 26 is allowable because none of the cited prior art references, either individually or in combination, expressly teach the following limitation in combination with the other limitations of claim 26:

> "... a third Flash memory portion not organized to emulate the EEPROM."

30. New Claim 27 depends from allowed Claim 26 and is therefore allowable.

Conclusion

31. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

32. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone numbers are (703) 306-0297 *[Before Oct. 25, 2004]* and (571) 272-3714 *[After Oct. 25, 2004]*. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached at (703) 305-9704 *[Before Oct. 25, 2004]* and (571) 272-3716 *[After Oct. 25, 2004]*.

Any response to this office action should be faxed to (703) 872-9306 or mailed to:

Director of Patents and Trademarks
Washington, DC 20231

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center 2100 Receptionist, whose telephone number is (703) 305-3900 *[Before Oct. 25, 2004]* or (571) 272-2100 *[After Oct. 25, 2004]*.

Ayal I. Sharon

Art Unit 2123

October 21, 2004